EMBEDDED BASED WIND PLANT MONITORING SYSTEM USING WIRELESS SENSOR NETWORK

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ABSTRACT:

This paper describes wireless sensor network for remote diagnosis and monitoring of a wind mill be a target application ,which is further grouped into small cluster and connected to the local server and communicate with remote server through internet. Here we are using the PIC 16F887 microcontroller and zigbee module and ARM7TDMI processor for diagnosis. The speed of the fan is sensed by using the RPM sensor, the current and voltage value generated is measured and the values are sent to the PIC controller for measure the import and export of wind power .Once the values are obtained in the controller a back up is stored and also the details are sent through wireless ZIGBEE communication medium so that the system can be operated by a personal computer located in a remote area connected through the internet. Similarly number of systems can be placed under control for monitoring as the number of pins and ports available in controller are more. The other end consists of a system which consists of an internet connection through which control can be made to the wind plant, the input information is obtained through the wireless ZIGBEE communication medium so that number of parameters can be obtained.

Keywords:

Wireless sensor, ZIGBEE Module, ARM7TDMI, PIC 16F877A Microcontroller,

Wind plant, GSM module, etc..,

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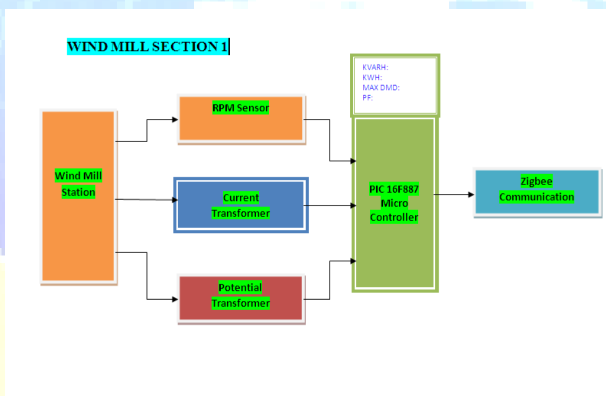
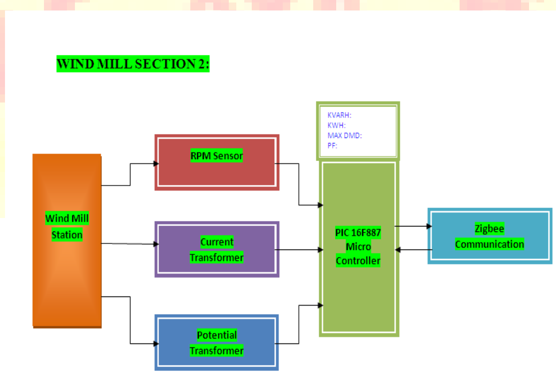
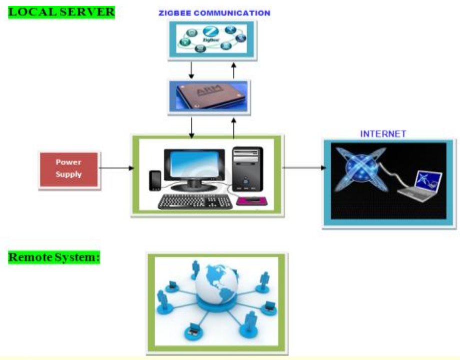
1. INTRODUCTION

The existing technology in India is wired that is uses fiber optics for controlling and monitoring wind mill operations. Due to complexity and drawbacks of the wired systems are changed into a wireless system in our modern global environment. The wired systems have some disadvantages like does not to be closed to monitored phenomenon and also the cost of and installing fiber optic cabling is relatively costly. In this paper we concentrate the wind power plant energy consumption details through the wireless sensor networks. In the existing design of wind power plant engineers must provided with the parameters like voltage ,current, frequency, wind speed , wind direction, speed of the rotor and power factor ,etc. The accurate collection of data from wind power generation mainly based on the collection of data and transmission interface and its relevant systems.

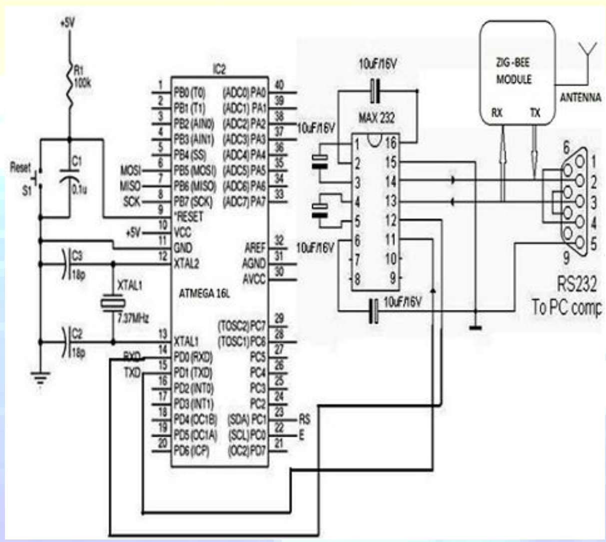
2. BLOCK DIAGRAM



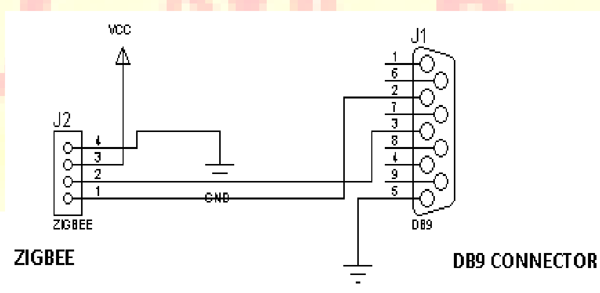




2. CIRCUIT DIAGRAM



Schematic of Measuring section (Transmitting Section)



Schematic of Data collection Section (Receiving Section)

3. HARDWARE DESIGN

PIC 16F877 features

High Performance RISC CPU:

• Only 35 single word instructions to learn

• All single cycle instructions except for program branches, which are two-cycle

• Operating speed: DC - 20 MHz clock input

DC - 200 ns instruction cycle

• 8K x 14 words of Program Memory

- 368 x 8 bytes of Data Memory (RAM)
- 256 x 8 bytes of EEPROM Data Memory

• Pin out compatible to PIC16F874A/877A

• Interrupt capability

• Eight-level deep hardware stack

• Direct, Indirect and Relative Addressing modes

Peripheral Features:

• High Sink/Source Current: 25 mA

• Timer0: 8-bit timer/counter with 8-bit prescaler

• Timer1: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock

• Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler

• Capture, Compare, PWM (CCP) module

- Capture is 16-bit, max. resolution is 12.5 ns

- Compare is 16-bit, max. resolution is 200 ns

- PWM max. resolution is 10-bit

• 10-bit, 8-channel analog-to-digital converter

• Synchronous Serial Port (SSP) with SPI™ (Master/Slave) and I2C™ (Slave)

• Brown-out detection circuitry for Brown-out Reset (BOR)

CMOS Technology:

• Low power, high speed CMOS FLASH technology

• Fully static design

• Wide operating voltage range: 2.0V to 5.5V

• Industrial temperature range

• Low power consumption:

- < 0.6 mA typical @ 3V, 4 MHz

- 20 A typical @ 3V, 32 kHz

- < 1 A typical standby current

Special Microcontroller Features:

• 1,000 erase/write cycle FLASH program memory typical

• Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)

• Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation

• Programmable code protection

• Power saving SLEEP mode

• Selectable oscillator options

• In-Circuit Serial Programming™ (ICSP™) via 2 pins

• Processor read access to program memory

ARM7TDMI:

The ARM7TDMI-S processor is a member of the ARM family of general-purpose 32-bit microprocessors. The ARM family offers high performance for very low-power consumption and gate count.

The ARM architecture is based on Reduced Instruction Set Computer(RISC) principles. The RISC instruction set, and related decode mechanism are much simpler than those of Complex Instruction Set Computer(CISC) designs. This simplicity gives:

• a high instruction throughput

• an excellent real-time interrupt response

• a small, cost-effective, processor macrocell

The instruction pipeline

The ARM7TDMI-S processor uses a pipelineto increase the speed of the flow of instructions to the processor. This enables several operations to take place simultaneously, and the processing, and memory systems to operate continuously. A three-stage pipeline is used, so instructions are executed in three stages:

• Fetch
• Decode
• Execute.

Memory access

The ARM7TDMI-S processor has a Von Neumann architecture, with a single 32-bit data bus carrying both instructions and data. Only load, store, and swap instructions can access data from memory. Data can be 8-bit bytes, 16-bit half words, or 32-bit words. Words must be aligned to 4-byte boundaries. Half words must be aligned to 2-byte boundaries.

Memory interface

The memory interface of the ARM7TDMI-S processor enables performance potential to be realized, while minimizing the use of memory. Speed-critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic. These control signals facilitate the exploitation of the fast-burst access modes supported by many on-chip and off-chip memory technologies.

The ARM7TDMI-S processor has four basic types of memory cycle:

• Internal cycle
• non sequential cycle
• Sequential cycle
• Coprocessor register transfer cycle.

ARM7TDMI-S architecture

The ARM7TDMI-S processor has two instruction sets:

• The 32-bit ARM instruction set
• The 16-bit Thumb instruction set.

The ARM7TDMI-S processor is an implementation of the ARM architecture v4T. Instruction compression Microprocessor architectures traditionally had the same width for instructions and data. Therefore, 32-bit architectures had higher performance manipulating 32-bit data and could address a large address space much more efficiently than 16-bit architectures. 16-bit architectures typically had higher code density than 32-bit architectures, and greater than half the performance.

Thumb implements a 16-bit instruction set on a 32-bit architecture to provide:

• higher performance than a 16-bit architecture

• higher code density thana 32-bit architecture.

The Thumb instruction set:

The Thumb instruction set is a subset of the most commonly used 32-bit ARM instructions. Thumb instructions are each 16bits long, and have a corresponding 32-bit ARM instruction that has the same effect on the processor model. Thumb instructions operate with the standard ARM register configuration, allowing excellent interoperability between ARM and Thumb states. On execution, 16-bit Thumb instructions are transparently decompressed to full 32-bit ARM instructions in real time, without performance loss.

Thumb has all the advantages of a 32-bit core:

• 32-bit address space

• 32-bit registers

• 32-bit shifter and Arithmetic Logic Unit (ALU)

• 32-bit memory transfer.

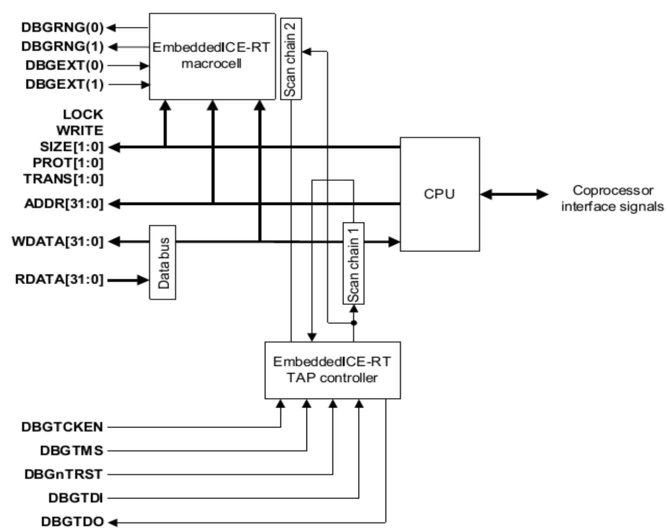


Figure - ARM7TDMI-S block diagram

Improved Debug Communications Channel (DCC) bandwidth

In the ARM7TDMI-S (Rev 3) processor, two accesses to scan chain 2 were required to read the DCC data. The first accessed the status bit, and the second accessed the data itself. To increase DCC bandwidth, only one access is required to read both the data and the status bit in the ARM7TDMI-S (Rev 4) processor. The status bit is now included in the least significant bit of the address field that is read from the scan chain. The status bit in the DCC control register is left unchanged to ensure backwards compatibility.

Access to DCC through JTAG

The DCC control register can be controlled from the JTAG interface in ARM7TDMI-S Rev 4. A processor write clears bit 0, the data read control bit.

Processor operating states

The ARM7TDMI-S processor has two operating states:

ARM state 32-bit, word-aligned ARM instructions are executed in this state. Thumb state 16-bit, half word-aligned Thumb instructions.

Memory formats

The ARM7TDMI-S processor views memory as a linear collection of bytes numbered in ascending order from zero:

• Bytes 0 to 3 hold the first stored word

• Bytes 4 to 7 hold the second stored word

• Bytes 8 to 11 hold the third stored word.

The ARM7TDMI-S processor can treat words in memory as being stored in one of: • Big-endian format

• Little-endian format.

Operating modes

The ARM7TDMI-S processor has seven operating modes:

• User mode is the usual ARM program execution state, and is used for executing most application programs.

• Fast interrupt (FIQ) mode supports a data transfer or channel process.

- Interrupt (IRQ) mode is used for general-purpose interrupt handling.
- Supervisor mode is a protected mode for the operating system.
- Abort mode is entered after a data or instruction pre fetch abort.
- System mode is a privileged user mode for the operating system.
- Undefined mode is entered when an undefined instruction is executed

The Thumb state register set

The Thumb state register set is a subset of the ARM state set. The programmer has direct access to:

- Eight general registers, r0–r7 the PC
- A Stack Pointer (SP)
- A Link Register (LR)
- The CPSR.

The relationship between ARM state and Thumb state registers

The Thumb state registers relate to the ARM state registers in the following way:

- Thumb state r0–r7, and ARM state r0–r7 are identical
- Thumb state CPSR and SPSRs, and ARM state CPSR and SPSRs are identical
- Thumb state SP maps onto ARM state r13
- Thumb state LR maps onto ARM state r14
- The Thumb state PC maps onto the ARM state PC (r15).

The control bits the bottom eight bits of a PSR are known collectively as the control bits.

They are the:

- Interrupt disable bits
- T bit
- Mode bits.

The control bits change when an exception occurs. When the processor is operating in a privileged mode, software can manipulate these bits.

Interrupt disable bits

The I and F bits are the interrupt disable bits:

- When the I bit is set, IRQ interrupts are disabled
- When the F bit is set, FIQ interrupts are disabled.

T bit

The T bit reflects the operating state:

• When the T bit is set, the processor is executing in Thumb state

• When the T bit is clear, the processor executing in ARM state.

The operating state is reflected by the CPTBIT external signal.

RPM SENSING USING MOC7811 :(SPEED SENSOR)

MOC7811 is a slotted Opto isolator module, with an IR transmitter & a photodiode mounted on it. Performs Non-Contact Object Sensing. This is normally used as positional sensor switch (limit switch) or as Position Encoder sensors used to find position of the wheel. It consists of IR LED and Photodiode mounted facing each other enclosed in plastic body.

SPECIFICATIONS

- Mounting hole diameter: 3mm
- Mounting hole spacing: 19mm
- Slot width: 3mm
- Slot depth: 7mm

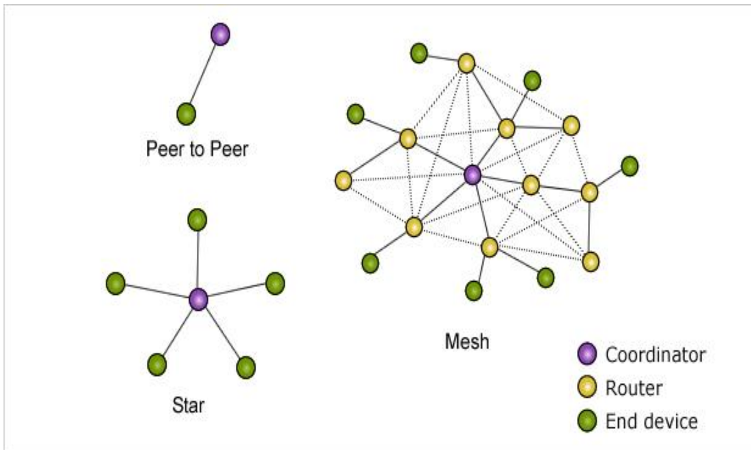
DETAILS

When light emitted by the IR LED is blocked because of alternating slots of the encoder disc logic level of the photo diode changes. This change in the logic level can be sensed by the microcontroller or by discrete hardware. This sensor is used to give position feedback to the robot or as Limit switches.

ZIGBEE NETWORKS:

It provides the most modern technology infrastructure for wireless devices. They are widely used in huge industrial plants but now spreading rapidly in home environment. ZIGBEE networks uses Coordinator, router (optional) and End Devices to communicate. In a ZIGBEE networking coordinators work as a primary device.

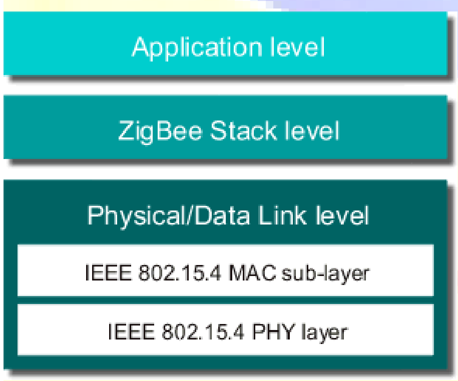
TYPES OF ZIGBEE NETWORKS :



ZIGBEE NETWORK FEATURES:

ZIGBEE Network speed- ZIGBEE technology presence in any device has a very exclusive feature of enabling the instant networking. ZIGBEE Network Capacity- ZIGBEE network has a capacity of connecting more than 65,000 devices ZIGBEE network Standards- The standard use in ZIGBEE networks is IEEE 802.15.4 . As compared to Bluetooth, ZIGBEE network covers a wide range from 10-40m

ZIGBEE Architecture:



Application Level:

The Application level contains the applications that run on the network node. These give the device its functionality - essentially an application converts input into digital data, and/or converts digital data into output. A single node may run several applications - for example, an environmental sensor may contain separate applications to measure temperature, humidity and atmospheric pressure.

ZIGBEE Stack Level:

The ZIGBEE Stack level provides the ZIGBEE functionality, and provides the glue between the applications and the Physical/Data Link level. It consists of stack layers concerned with network structure, routing and security (encryption, key management and authentication).

Physical/Data Link Level:

The Physical/Data Link level is concerned with low-level network operation such as addressing and message transmission/reception. It is based on the IEEE 802.15.4 standard and comprises the following two layers:

MAC (Media Access Control) sub-layer

PHY (Physical) layer

DEVICE TYPES:

The coordinator forms the root of the network tree and might bridge to other networks. There is exactly one ZIGBEE coordinator in each network. It is able to store information about the network ZIGBEE Router (ZR): a router can act as an intermediate router, passing on data from other devices. ZIGBEE End Device (ZED): Contains just enough functionality to talk to the parent node (either the coordinator or a router). A ZED requires the least amount of memory, and therefore can be less expensive to manufacture than a ZR or ZC

ZIGBEE CHARACTERISTIC:

Low power consumption Maximum data rates allowed for various frequency bands High throughput and low latency (0.1 %) Channel access using Carrier Sense Multiple Access with Collision Avoidance (CSMA – CA) Addressing space of up to 64 bit IEEE address devices, 65,535 networks

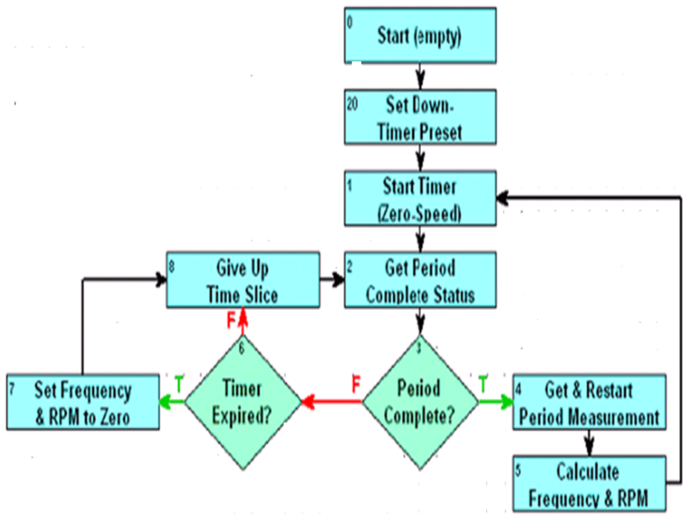
ADVANTAGES:

- Low cost Range and obstruction issues avoidance Multi-source products.
- Low power consumption.

DISADVANTAGES:

- Cost still high Total solutions still lacking – slow to materialize Not widely spread.

Sensing algorithm:



2. OPERATION

In this project the wind mill section consist of a generator where the power generated will be extracted and the corresponding parameters like current speed of the wind mill section, input and output voltage will be monitored. These information's will be sent to the controller, the controller chosen for this project is PIC 16F887 microcontroller which has numerous ports so that number of inputs can be given or connected. The collected information will be processed and then the individual wind mill section will be sent to the remote server for the corresponding area through a wireless communication medium which is the ZIGBEE communication.

Numbers of windmills are connected to a local area server, each server can be connected through internet connection using GSM communication module. The server systems consist of ARM 7TDMI processor it is also attached with a internet connection for data transmission and reception. The details can also be stored in personal computer as a database and can be used in future for further reference.

The ARM processor and the PIC controller is simultaneously used here for monitoring and controlling the wind power generation mechanism where the operations can be controlled even from the remote server. If any problems are encountered in the wind mill unit, the problems will be analyzed in internet and proper solution like controlling the speed or rotation of the blades, generator repair through manual means can be allotted for individual sectors.

3. RESULTS

A low-cost solution to enhance the remote monitoring capability of wind mill system is proposed. Windmill system for monitoring voltage and current of wind –electricity generator is designed and developed at lab scale and found that

(1)It is secure, robust and low-power consuming.

(2)It can operate on multiple channels to avoid interference with other wireless devices (5) Continuous monitoring can help fault detection of particular wind mill in wind farm. The proposed system will provide a method to investigating the behavior of each windmill and will reduce the monitoring cost. Again different sensors for the measurement of parameters like wind speed, temperature, and humidity, will be interfaced for correlation and investigation of the effect of environmental loads. This method can also be applied to energy generation like Solar, Fuel cells, Hydroelectric etc. and they can be monitoring by utilizing heterogeneous wireless personal area networks.

4. CONCLUSION

From the above designed project we can conclude that the wireless sensor network that can be used for windmill monitoring. Wireless technology, zigbee can be used for applications. The aim of developing this wireless windmill monitoring system was to design a system for conditional monitoring of windmill, that can gather various parameters such as voltage, current, speed etc. using sensors or devices, transmit that recorded data wirelessly to the base station, display the transmitted data on a screen and providing shut down if the system detects an equipment failure, all without human intervention.

REFERENCE

1.Energy Conscious Application of ZigBee Wireless Networks in Machine Health MonitoringSystems.-HalitEren,SMIEEEDepartment of Electrical and Computer EngineeringCurtin University, Perth, WA, Australia.

2. **Online and Remote Motor Energy Monitoring and Fault Diagnostics Using Wireless Sensor Networks** -Bin Lu, *Senior Member, IEEE*, and Vehbi C. Gungor, *Member, IEEE*

3.**Concept of Low-Cost Energy Monitoring System for Household Application-** Peteris Apse-Apsitis, Ansis Avotins, Leonids RibickisRiga Technical University, Kronvalda boulevard 1 – 315, LV-1010, Riga, Latvia*peter*.

4.**Ad hoc Sensor for Windmill Conditiong Monitoring and control**-Trupti A.Nawadar , TenaEngineering collage , Navi Numbai,India.

5. ‘**Design of micro generation monitoring and control application.** ‘Lehtla .M., Koivastik,L., Moller,t., Kalliaste,A.,and Rosin A(2010) elelctric power quality and supply reliability conference kuressaare.,

6.**Wireless network architecture for diagnosis and monitoring applications**.-Zeashan hammeed Khan , Jean Marc Thiriet ,consumer communications and networking conference 2009, Las Vegas ,United States.

7. **David A. Spera: Wind Turbine Technology, ASME Press (1994)**.

8. **F.L.Lewis “Wireless Sensor Networks”- Chapter 4, Smart environments: Technologies, Protocols**, and Applications Journal.

Websites.

1.www.wikipedia.org

2.www.keil.com

3.www.circuitlake.com